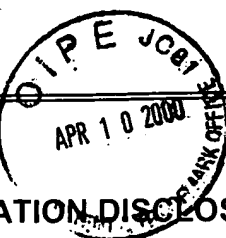


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INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Applicant: Yashuhiko TAKEMURA et al.

Filing Date: May 28, 1999

Group: 2822

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
<i>W</i>	5,091,334	2/25/92	Yamazaki et al.	437	101	3/5/90
<i>W</i>	5,262,350	11/16/93	Yamazaki et al.	437	170	7/1/92
<i>W</i>	5,591,987	1/7/97	Yamazaki et al.	257	57	8/14/92
<i>W</i>	5,543,352	8/6/96	Ohtani et al.	437	101	11/16/94
<i>W</i>	5,585,291	12/17/96	Ohtani et al.	437	40	11/29/94
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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>W</i>	Stanley Wolf., Ph.D, et al. "Silicon Processing for the VLSI ERA", vol. 1: process technology, Lattice Press, pp. 216-218

Examiner:

Yung A. Lin

Date Considered:

06/00

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